PowerPC™

Errata to
MPC750 RISC Microprocessor User's Manual

This errata describes corrections to the *MPC750 RISC Microprocessor User's Manual*. These corrections also apply to the MPC740, which is described in *MPC750 RISC Microprocessor User's Manual*. For convenience, the section number and page number of the errata item in the user's manual are provided.

To locate any published updates for this document, refer to the world-wide web at http://www.mot.com/powerpc.

Section/Page	Changes
2.1.1, 2-7	The implementation note for the decrementer register (DEC) should read as follows: In the MPC750 the decrementer register is decremented and the time base is incremented at a speed that is one-fourth the speed of the bus clock.
2.1.2.2, 2-9	In Table 2-4, replace the description of HID0[DBP] (bit 1), with the following:

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1	DBP	Disable 60x bus address and data parity generation. 0 The system generates address and data parity. 1 Parity generation is disabled and parity signals are driven to 0 during bus operations. When parity generation is disabled, all parity checking should also be disabled and parity signals need not be connected.

Replace the description of HID0[BTIC] (bit 26), with the following:

26	BTIC	BTIC enable. Used to enable use of the 64-entry branch instruction cache. 0 The BTIC contents are invalidated and the BTIC behaves as if it were empty. New entries cannot be added until the BTIC is enabled. 1 The BTIC is enabled and new entries can be added.

2.1.2.4.5, 2-18 Replace Table 2-11 with the following:

Table 2-11. PMC2 Events—MMCR0[26–31] Select Encodings

Encoding	Description
00 0000	Register holds current value.
00 0001	Counts processor cycles.
00 0010	Counts completed instructions. Does not include folded branches.
00 0011	Counts transitions from 0 to 1 of TBL bits specified through MMRC0[RTCSELECT]. 00 = 47, 01 = 51, 10 = 55, 11 = 63.
00 0100	Counts instructions dispatched. 0, 1, or 2 instructions per cycle.
00 0101	Counts L1 instruction cache misses.
00 0110	Counts ITLB misses.
00 0111	Counts L2 instruction misses.
00 1000	Counts branches predicted or resolved not taken.
00 1001	Counts MSR[PR] bit toggles.
00 1010	Counts times reserved load operations completed.
00 1011	Counts completed load and store instructions.
00 1100	Counts snoops to the L1 and the L2.
00 1101	Counts L1 cast-outs to the L2.
00 1110	Counts completed system unit instructions.
00 1111	Counts instruction fetch misses in the L1.
01 0000	Counts branches allowing out-of-order execution that resolved correctly.
All others	Reserved.

2.1.5, 2-26 In Table 2-18, replace the description of L2CR[L2SL] (bit 16) with the following:

16	L2SL	L2 DLL slow. Setting L2SL increases the delay of each tap of the DLL delay line. It is intended to increase the delay through the DLL to accommodate slower L2 RAM bus frequencies. Generally, L2SL should be set if the L2 RAM interface is operated below the value specified in the *MPC750 Hardware Specifications*.

2.3.4.3.10, 2-52 Add the following footnote for the **stfd** instruction in Table 2-39

Each FPR has additional internal bits associated with them that specify the type of floating-point number that the register contains. These bits are set properly whenever the FPR is loaded. However, at power up, the FPR may be misinterpreted as containing a denormalized number, with the mantissa containing all zeros. If an **stfd** is executed before the internal bits are corrected by a floating-point load operation, the part hangs while searching for a leading 1 in the mantissa.

To avoid this problem, upon coming out of a power-on reset, initialize all FPRs to be used. The value used for initialization is not important.

2.3.6.3.2, 2-67 Add the following note as a footnote to the **mtsr** and **mtsrin** instructions in Table 2-59:

Data page address translations that attempt to read a segment register (SR) during the same cycle a **mtsr** or **mtsrin** instruction is writing to any of the SRs causes the translation mechanism to receive the written data instead of the contents of the intended SR. This can occur if no context synchronizing instruction is between the **mtsr** or **mtsrin** and a succeeding data address translation that use any SR.

This problem can, within specific timing windows, cause the incorrect segment data to be used for translation under these circumstances. Instruction address and block address translations are not susceptible to this problem.

To avoid this problem, a context-synchronizing instruction, such as an **isync**, should be placed between any **mtsr**/**mtsrin** instructions and succeeding instructions that cause a data address translation that uses an SR.

3.4.2.2, 3-16 Add the following to the end of the section:

If the target address of a **dcbz** instruction hits in the L1 cache, the MPC750 requires four internal clock cycles to rewrite the cache block to zeros. On the first clock, the block is remarked as valid-unmodified, and on the last clock the line is marked as valid-modified. If a snoop request to that address is received during the middle two clocks of the **dcbz** operation, MPC750 does not properly react to the snoop

	operation or generate an address retry (by an $\overline{\text{ARTRY}}$ assertion) to the other master. The other bus master continues reading the data from system memory, and both the MPC750 and the other bus master end up with different copies of the data. In addition, if the other bus master has a cache, the cache block is marked valid in both caches, which is not allowed in MPC750's three-state cache environment. For this reason, avoid using **dcbz** for data that is shared in real time and that is not protected during writing through higher-level software synchronization protocols (such as semaphores). Use of **dcbz** must be avoided for managing semaphores themselves. An alternative solution could be to prevent **dcbz** from hitting in the L1 cache by performing a **dcbf** to that address beforehand.
4.5.11, 4-20	Remove Table 4-10, "Trace Exception—SRR1 Settings." This interrupt is implemented as defined by the OEA. Remove the Table 4-10 and the introductory text.
5.1.7, 5-18	Table 5-4, delete the second row in table (**lwarx** or **stwcx.** with W = 1).
5.1.8, 5-19	In Table 5-5, remove the next-to-last paragraph ("In addition, depending...") from the **tlbie** description.
5.4.3.1, 5-26	The next-to-last paragraph should read as follows: To uniquely identify a TLB entry as the required PTE, the TLB entry also contains four more bits of the page index, EA[10–13] (in addition to the API bits in the PTE).
5.4.3.1, 5-27	The second sentence in the second paragraph should read as follows: ITLB miss exception conditions are reported when there are no more instructions to be dispatched or retired (the pipeline is empty).
5.4.4, 5-29	Figure 5-8 in the published manual incorrectly shows the loopback arrow on the left side pointing to the node above the word 'Otherwise'. Replace Figure 5-8 with the following:

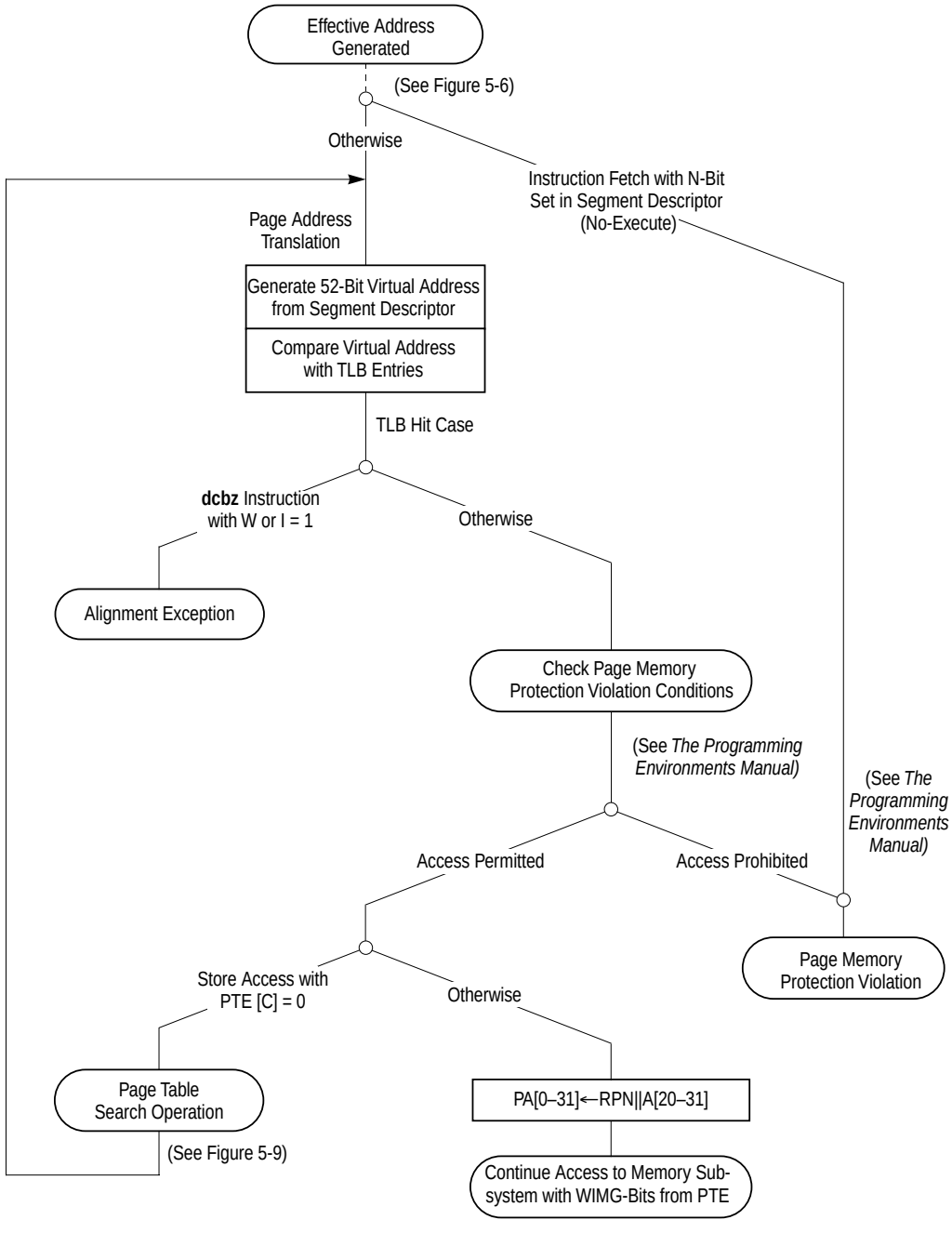
Effective Address Generated
(See Figure 5-6)
Otherwise
Instruction Fetch with N-Bit Set in Segment Descriptor (No-Execute)
Page Address Translation
Generate 52-Bit Virtual Address from Segment Descriptor
Compare Virtual Address with TLB Entries
TLB Hit Case
dcbz Instruction with W or I = 1
Otherwise
Alignment Exception
Check Page Memory Protection Violation Conditions
(See The Programming Environments Manual)
(See The Programming Environments Manual)
Access Permitted
Access Prohibited
Page Memory Protection Violation
Store Access with PTE [C] = 0
Otherwise
Page Table Search Operation
(See Figure 5-9)
PA[0–31]←RPN||A[20–31]
Continue Access to Memory Sub-system with WIMG-Bits from PTE

Figure 5-8. Page Address Translation Flow—TLB Hit

7.2.5.2.1, 7-14 For $\overline{\text{ARTRY}}$, change "Timing Comments," "Negation," first paragraph, last sentence to the following:

First the buffer goes to high impedance for a minimum of one-half processor cycle (dependent on the clock mode), then it is driven negated for one-half bus cycle before returning to high impedance.

8.3.1, 8-12 An overbar is missing for $\overline{TS}$ in the last sentence in the paragraph.

9.1.2, 9-5 In Table 9-1, replace the description of L2CR[L2DO] (bit 9), with the following:

9	L2DO	L2 data-only. Setting L2DO inhibits the caching of instructions in the L2 cache. All accesses from the L1 instruction cache are treated as cache-inhibited by the L2 cache (bypass L2 cache, no L2 tag look-up performed).

In Table 9-1, replace the description of L2CR[L2SL] (bit 16) with the following:

16	L2SL	L2 DLL slow. Setting L2SL increases the delay of each tap of the DLL delay line. It is intended to increase the delay through the DLL to accommodate slower L2 RAM bus frequencies. Generally, L2SL should be set if the L2 RAM interface is operated below the value specified in the *MPC750 Hardware Specifications*.

9.1.4, 9-7 Add the following to the end of the section:

If dynamic power management is enabled (HID0[DPM] = 1), a global invalidate of the L2 cache may not properly invalidate the L2 tag memory during the time that the L1's data cache is waiting for reload data to be received from system memory. During that time, circuity in the L1 data cache is stopped to conserve power, which inadvertently affects the state machine performing the L2 global invalidate operation.

There are two ways to avoid this:

- Be sure DPM = 0 during an L2 cache global invalidation.
- Ensure that the processor is in a tight uninterruptable software loop monitoring the end of the global invalidate, so that an L1 data cache miss cannot occur that would initiate a reload from system memory during the global invalidate operation.

11.2.1.5, 11-7 Replace Table 11-6 with the following:

Table 11-6. PMC2 Events—MMCR0[26–31] Select Encodings

Encoding	Description
00 0000	Register holds current value.
00 0001	Counts processor cycles.
00 0010	Counts completed instructions. Does not include folded branches.

Table 11-6. PMC2 Events—MMCR0[26–31] Select Encodings

Encoding	Description
00 0011	Counts transitions from 0 to 1 of TBL bits specified through MMRC0[RTCSELECT]. 00 = 47, 01 = 51, 10 = 55, 11 = 63.
00 0100	Counts instructions dispatched. 0, 1, or 2 instructions per cycle.
00 0101	Counts L1 instruction cache misses.
00 0110	Counts ITLB misses.
00 0111	Counts L2 instruction misses.
00 1000	Counts branches predicted or resolved not taken.
00 1001	Counts MSR[PR] bit toggles.
00 1010	Counts times reserved load operations completed.
00 1011	Counts completed load and store instructions.
00 1100	Counts snoops to the L1 and the L2.
00 1101	Counts L1 cast-outs to the L2.
00 1110	Counts completed system unit instructions.
00 1111	Counts instruction fetch misses in the L1.
01 0000	Counts branches allowing out-of-order execution that resolved correctly.
All others	Reserved.

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